Nanostencil Lithography and Nanoelectronic Applications

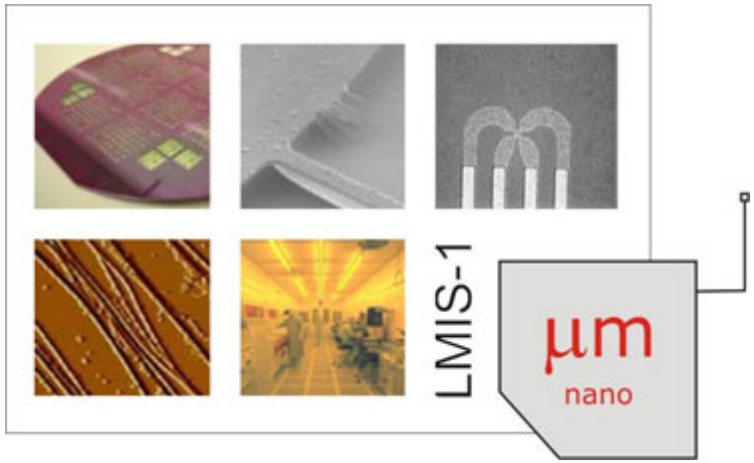
Oscar Vazquez, Marc van den Boogaart, Dr. Lianne Doeswijk, Prof. Juergen Brugger , *LMIS1*
Dr. Chan Woo Park, *Visiting Professor*
Dr. G.M. Kim, D. Grogg, *Former members*

Laboratoire de Microsystèmes
Ecole Polytechnique Fédérale
de Lausanne (EPFL)
Switzerland

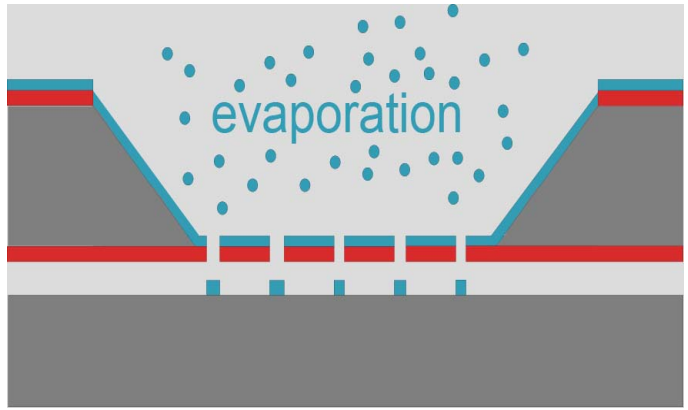
ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Outline

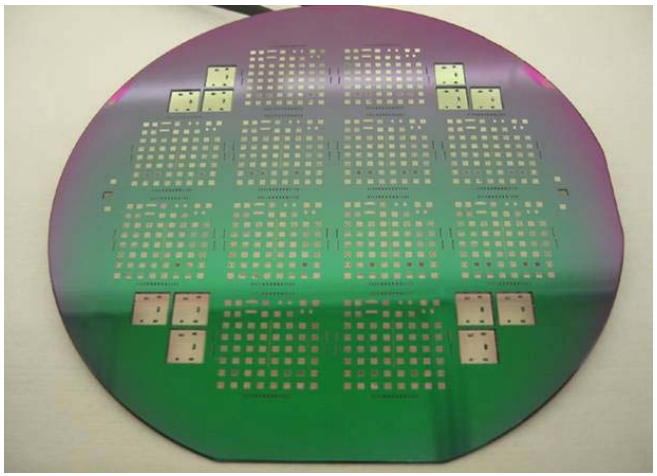
1. LMIS1 Activities



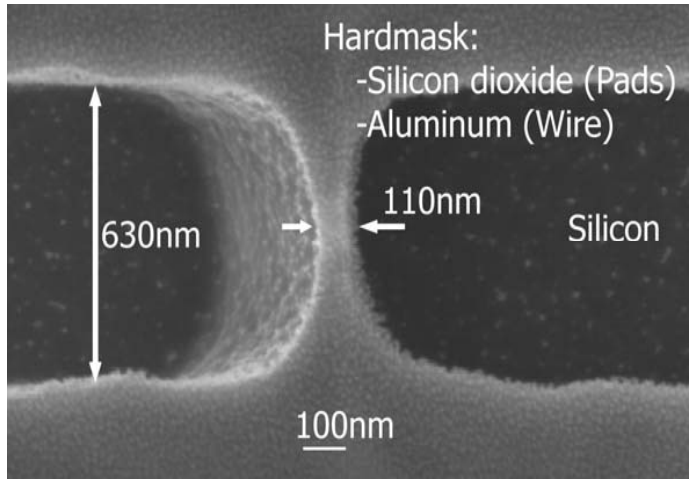
2. Nanostencil Technique



3. Challenges & Development



4. Nanoelectronics



LMIS 1 Microsystems and Nanoengineering

- Integration of micro and nanotechnologies into functional and advanced devices
- Alternative technologies to achieve sub-micron resolution at low-cost and with high throughput
- Integration of life-science technologies with current fabrication technologies for Lab-on-Chip devices.

LMIS 1 Microsystems and Nanoengineering

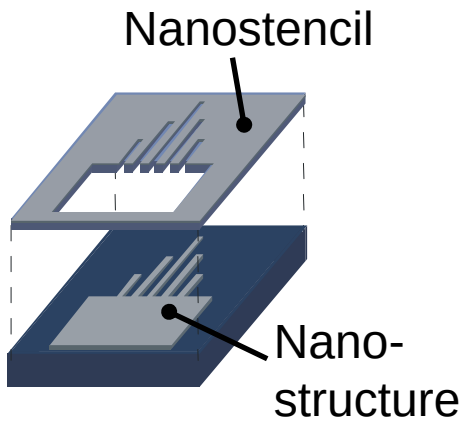
Micro/ Nanopatterning

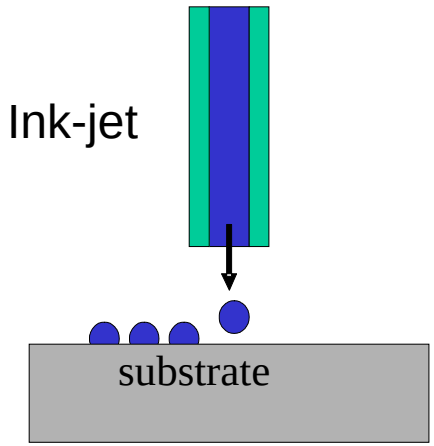
Micro/Nanostencil

FIB patterning

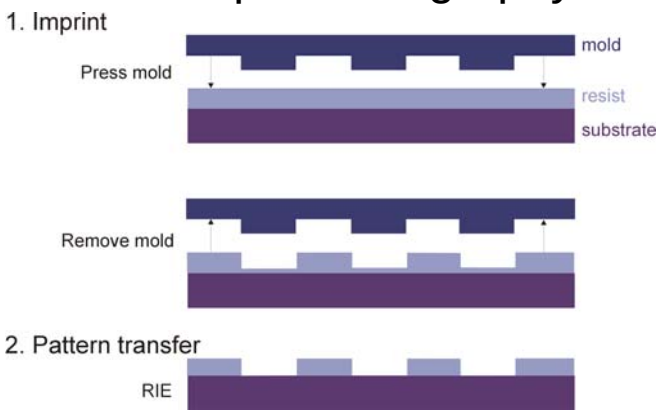
Ink-jet

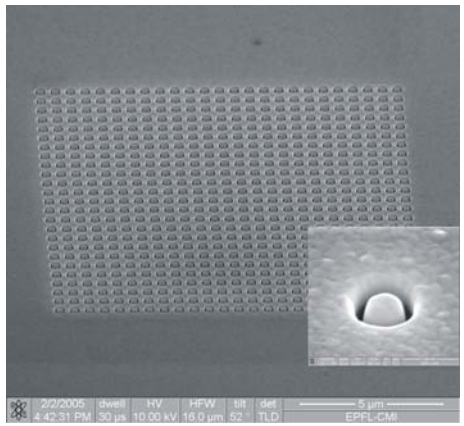
NIL





Nanoimprint lithography





FIB patterning

LMIS 1 Microsystems and Nanoengineering

Nanoprobes

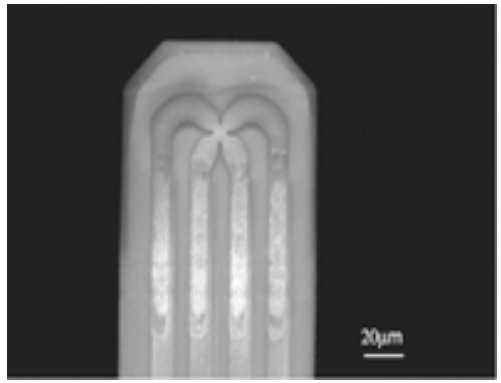
Metal AFM (W, Pt)

NanoHall

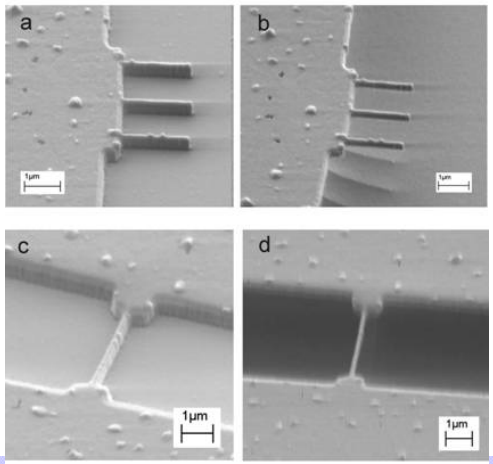
MRFM

NEMS

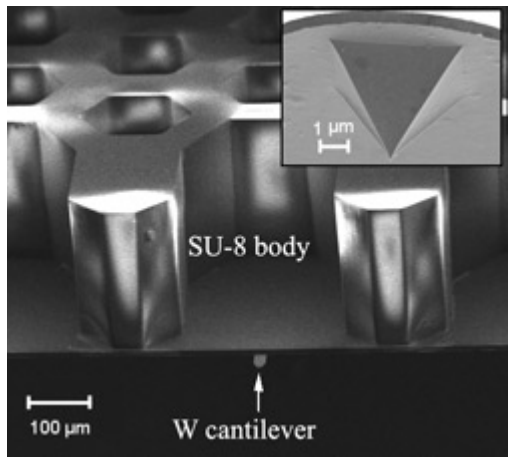
Bismuth Hall sensor



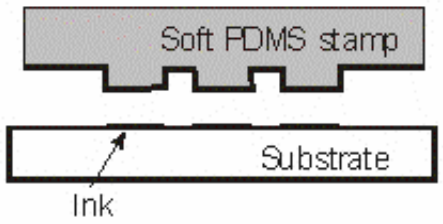
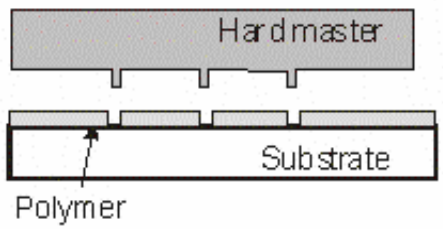
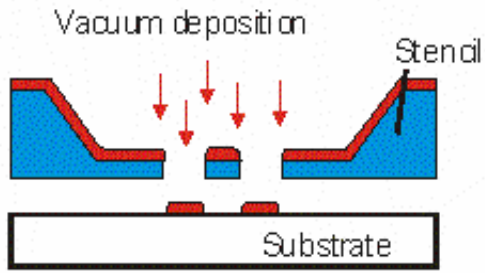
NEMS

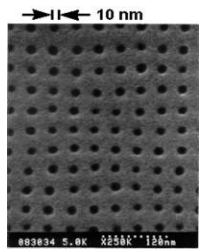


Conducting AFM probes

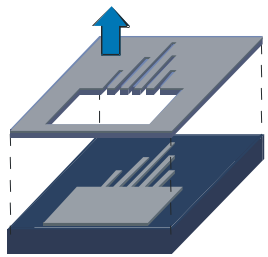


Emerging Patterning Methods

Soft-lithography	Nanoimprint lithography	Nanostencil lithography
Ink delivery molecules, wet *soft-contact*	Thermo-mechanical, nano-imprinting, *hard contact*	Local deposition stencil, vacuum *no contact*
		



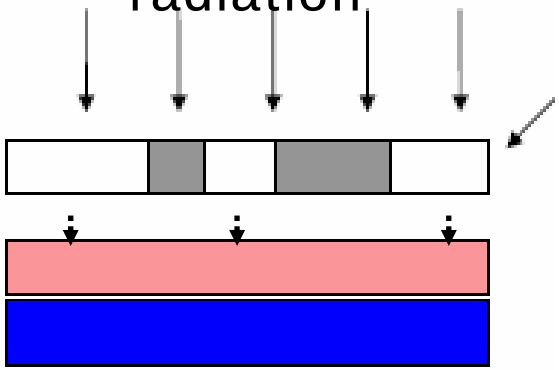
10 nm
Candidate for
Integrated Circuit



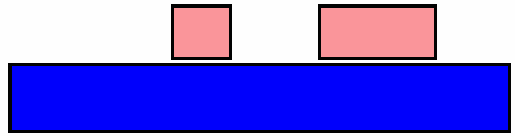
Photolithography

1.Cover substrate with photoresist

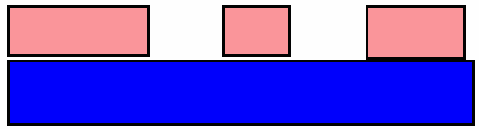
2. Exposure with Light radiation



3.- Development



Positive



Negative

Etching

By etching, materials like Silicon, SiO_2 can be patterned.
Lift-Off is also used to make metallic patterns

1

deposit thin film of desired material

2

coat and pattern photoresist

3

etch film using photoresist as mask

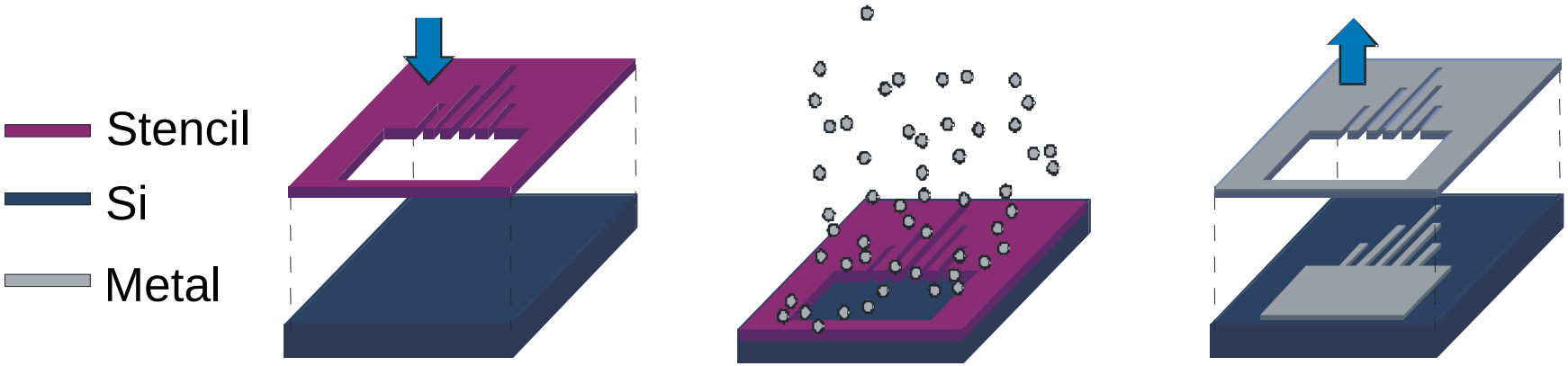
4

remove photoresist

Stencil technique

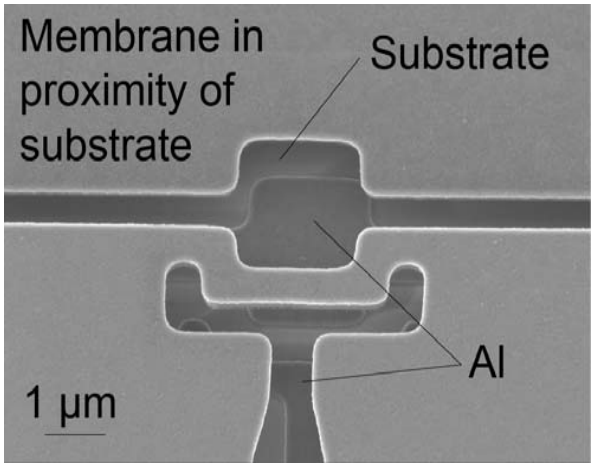
The Nanostencil technique is a patterning method based on shadow mask evaporation.

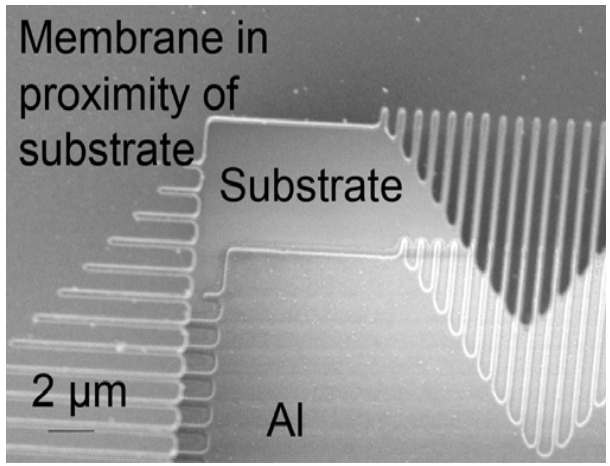
A thin membrane is used as a solid mask to transfer the patterns from the membrane to the substrate during the evaporation

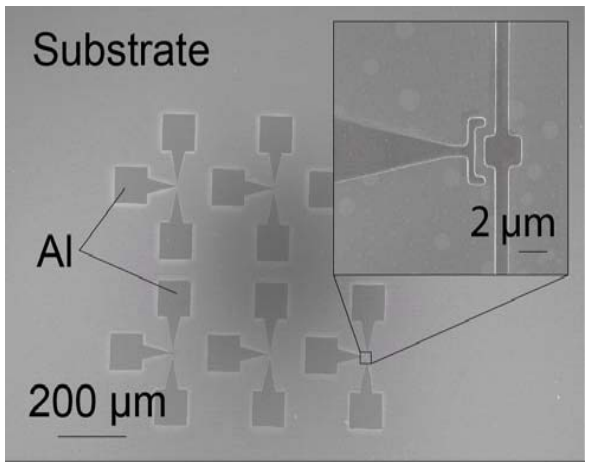


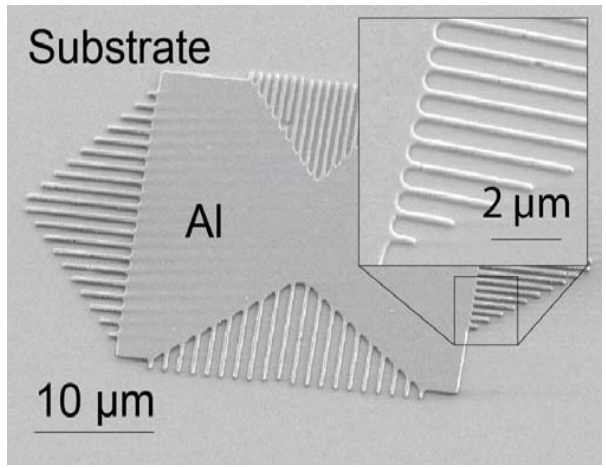
Basic Principle

Examples









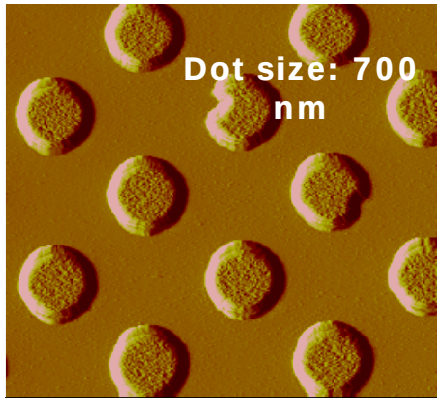
Top images:

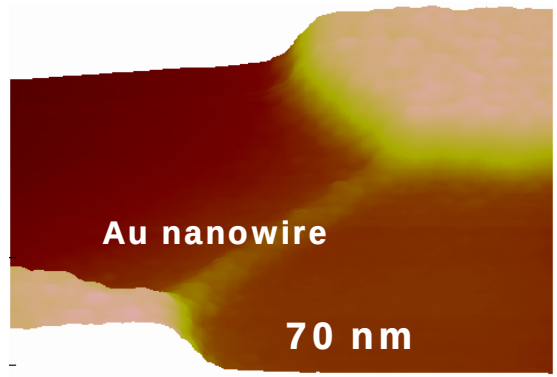
Stencil and substrate after evaporation

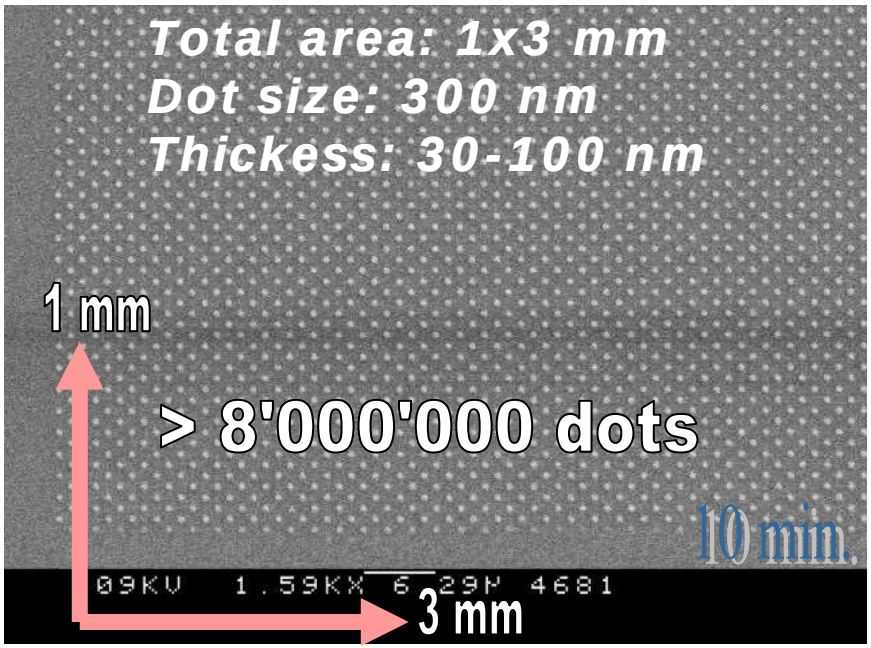
Bottom images:

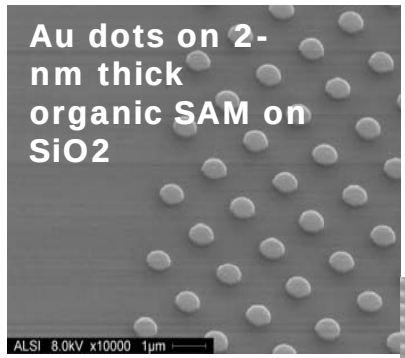
Resulting micro/nano structures after removal of stencil

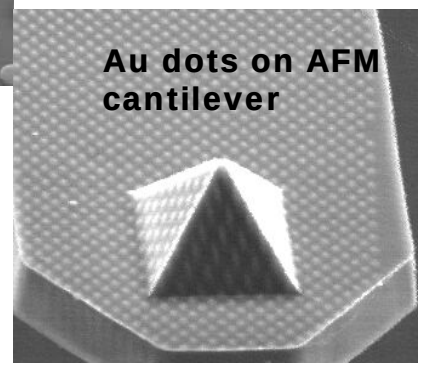
Examples











J. Brugger et al., Microelectronic Engineering 53 (2000) 403-405

Simple process

Stencil method is much simpler since it does not need any photoresist treatment

Photolithography

Spin coating of photoresist

Thermal baking

Exposure

Development

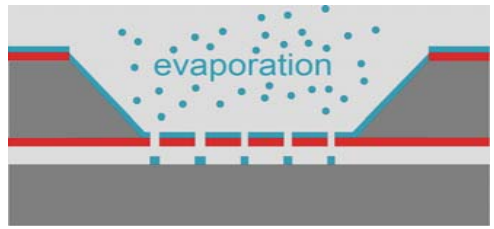
Evaporation

Lift-Off

Stencil method

Mount and align

Deposition through stencil



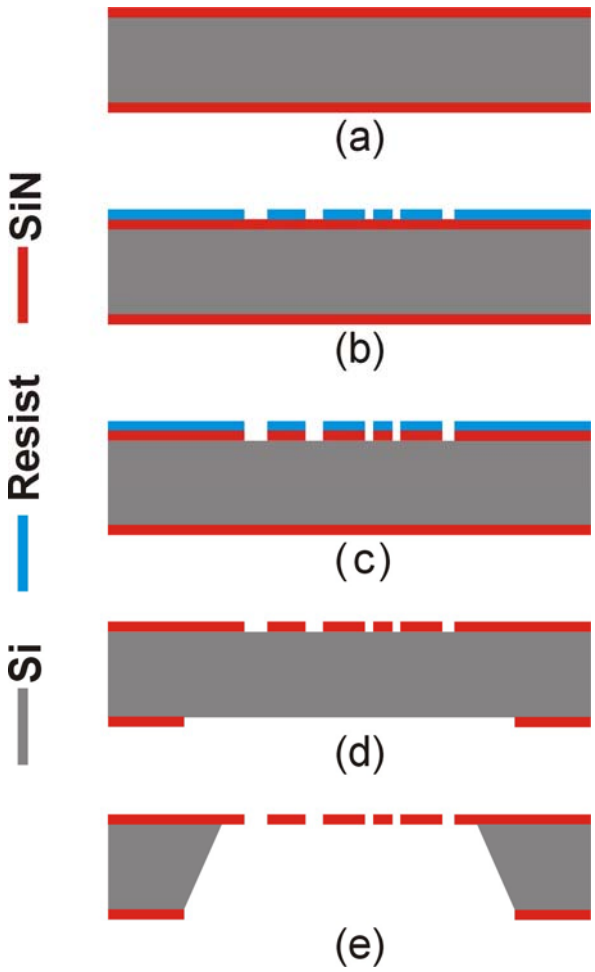
Main advantages

- No resist, development or baking → Clean and Soft technology
- Non-contact → Prepatterned, Fragile, non-planar, functionalized, CMOS, MEMS substrates
- Re-usable → Rapid and low-cost patterning
- Micro and nanostructuring in a single step → Wide range of size features
- High Flexibility of materials → Metals, Oxides (PLD), Piezoelectrics (PLD), SAMs

Potential Applications

- Nanoelectronics (High throughput with <1um nanometer resolution)
- Nanobiotechnology (Patterning of Inorganic-Organic interfaces)
- Nanoscale material science (High flexibility of materials)
- Sensors

Fabrication of the Stencil



→ LPCVD 100-500 nm Si_3N_4

→ Pattern definition by UV, FIB, E-Beam, Deep UV, Laser Int

→ Pattern transfer into Si_3N_4

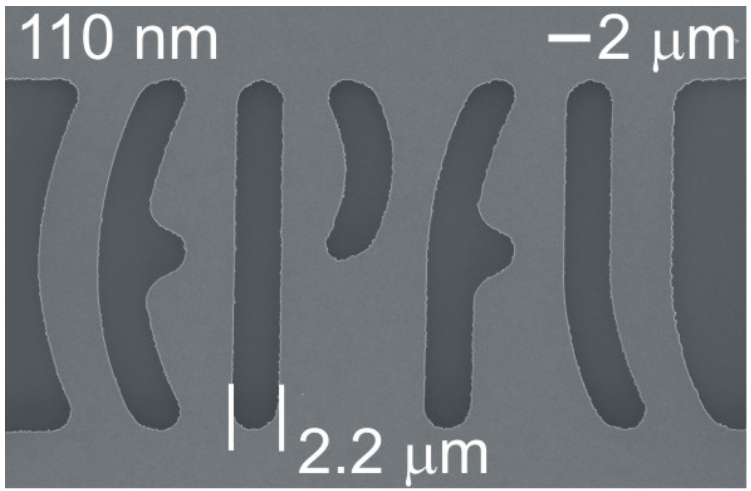
→ Backside lithography to define membranes' size

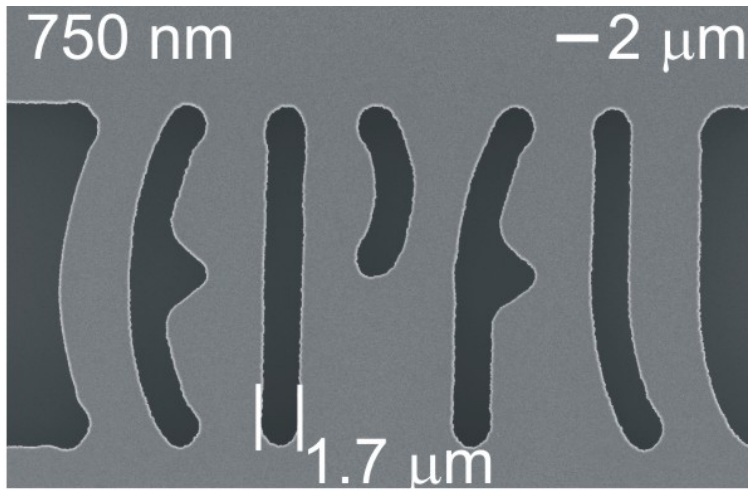
→ Membrane release by KOH

Challenges: Clogging

Clogging occurs due to the accumulation of deposited material on top and inside the membrane apertures.

Features' size is reduced as the material is evaporated.

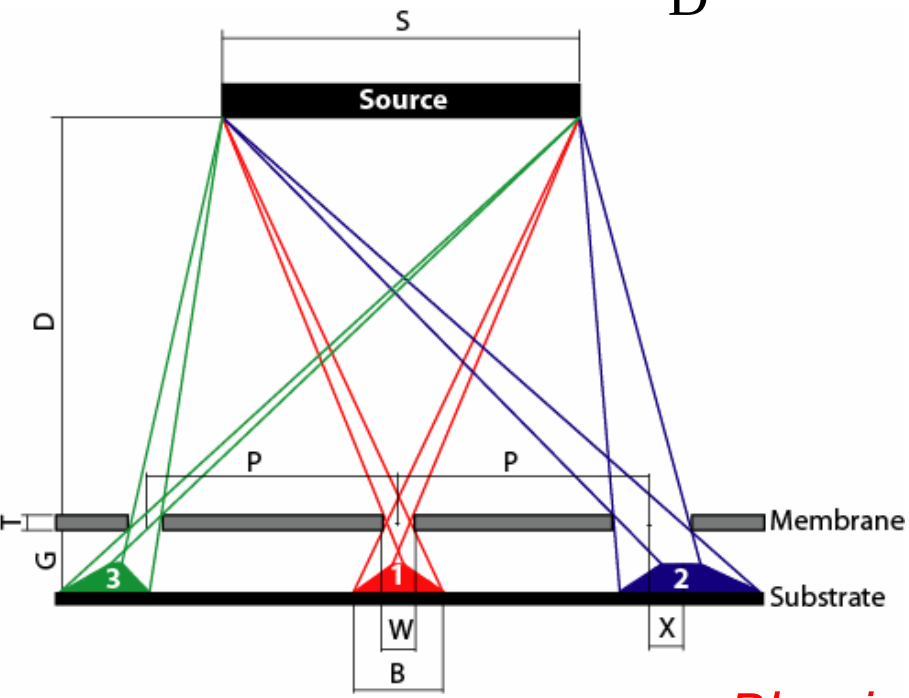




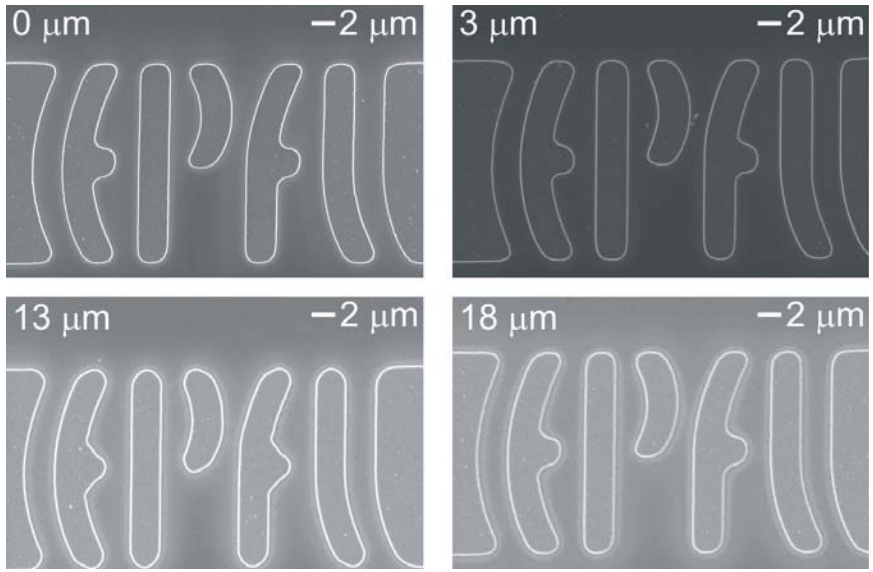
Challenges: Blurring

S >> W :

$$B = W + 2S_b \approx W + \frac{G \times S}{D}$$

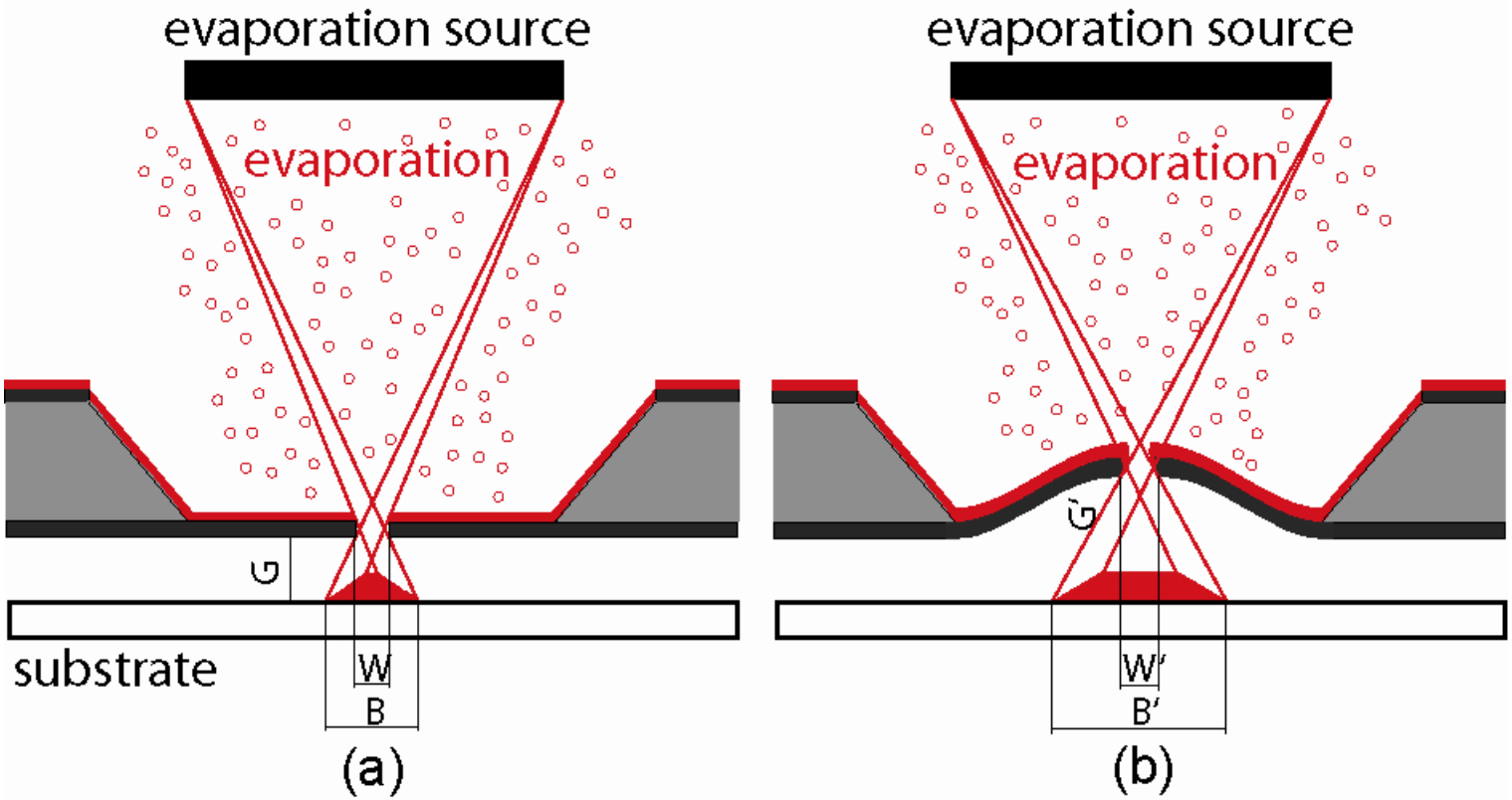


Size goes from 2.5 um up to 3 um as we the gap is increased



Blurring: Geometry, Diffusion and Evaporation method.

Challenges: Deformation



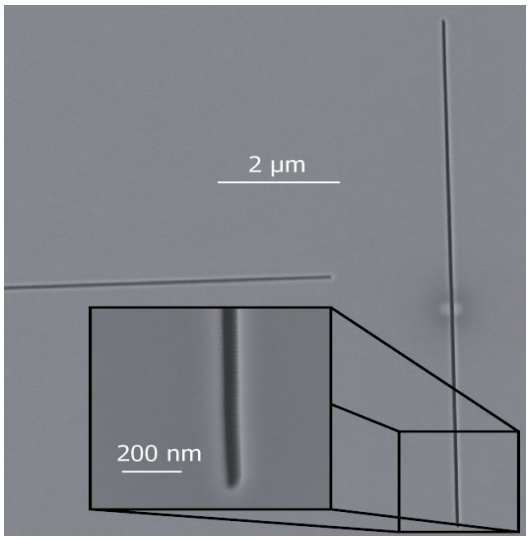
The deformed membrane induces both an increased gap and an altered aperture shape.

Main achievements

Nanostencils

(FIB)

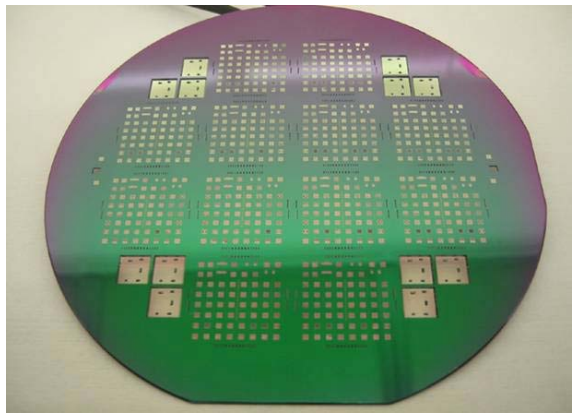
Nanoslits and Rapid Prototyping



Full-wafer stencils

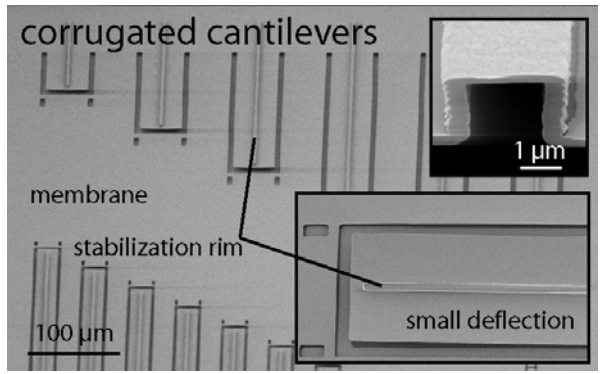
(DUV/MEMS)

High Throughput with Micro - and Nanometer apertures

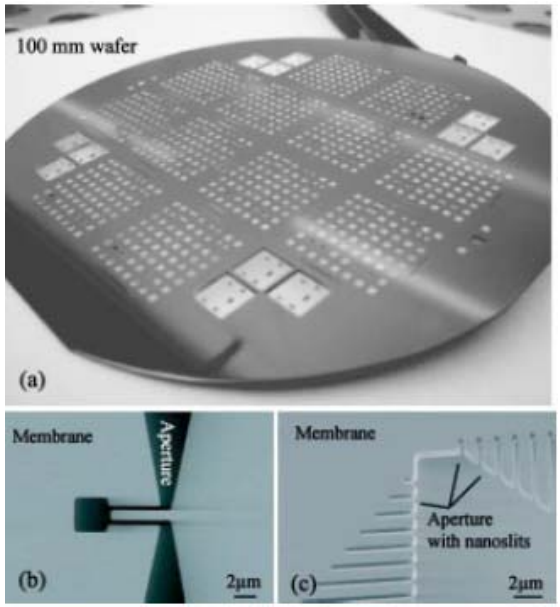


Stabilized stencils

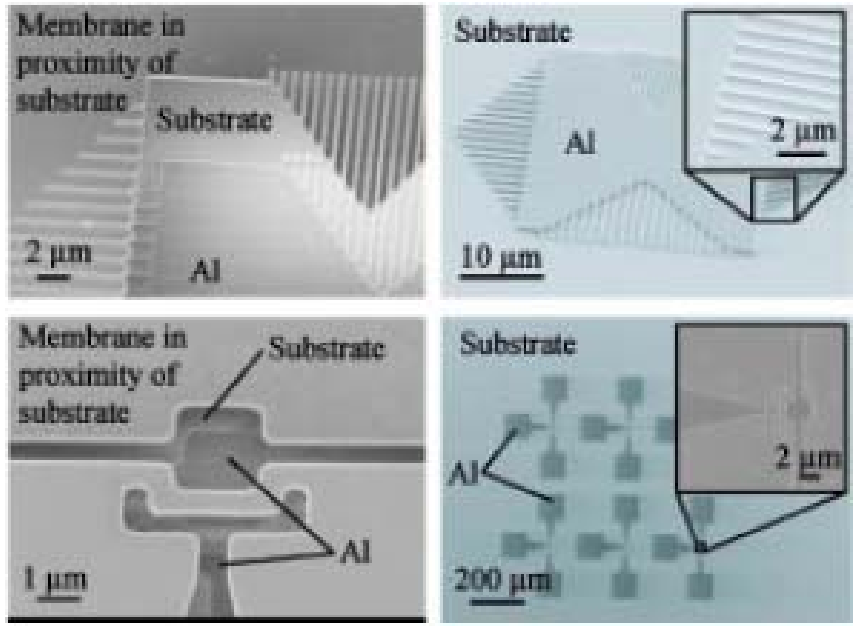
Deformation reduced up to 96%



Full wafer stencil with DUV



Full 4˝ wafer stencil with micro and nanometer apertures



Features from 200 nm up to 300 um were transfered into a substrate in a single evaporation step

HIGH THROUGHPUT!!

Reinforced Stencils

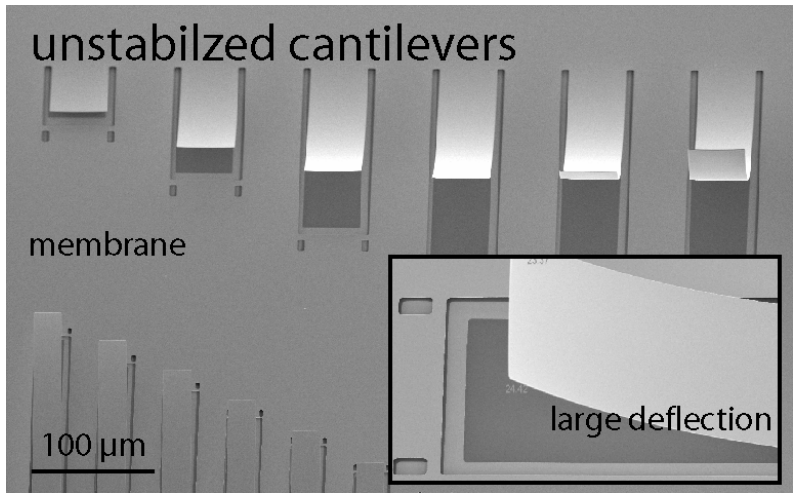
Use rims to increase the stiffness of the membrane

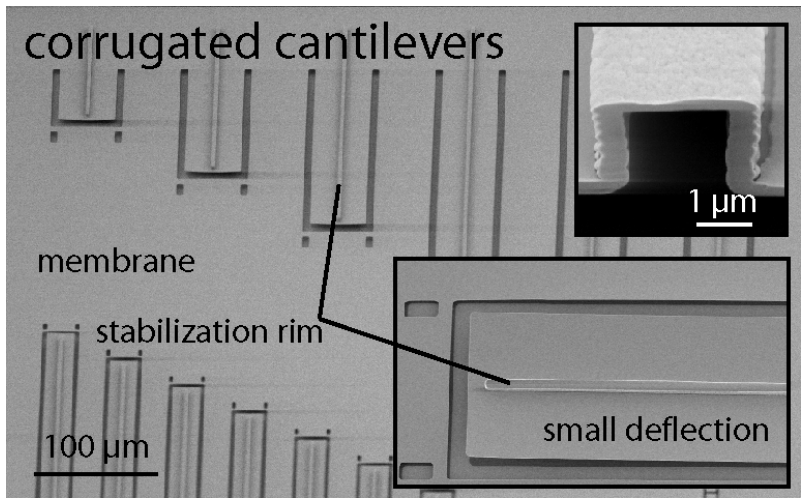
Top image:

- Cantilever-like membranes.
- Large deflection due to deposition induced stress

Bottom image:

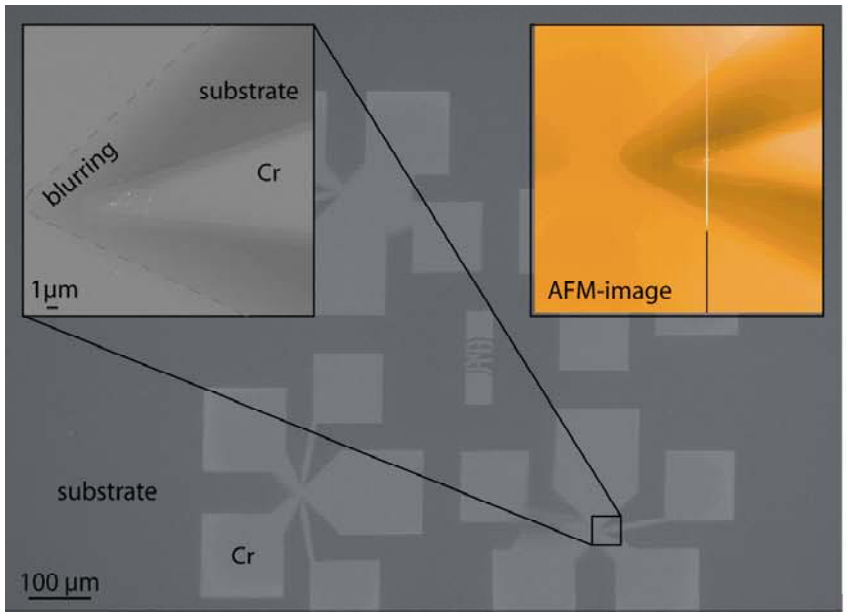
- Stabilized cantilever-like membranes.
- Small deflection due to stabilization rims



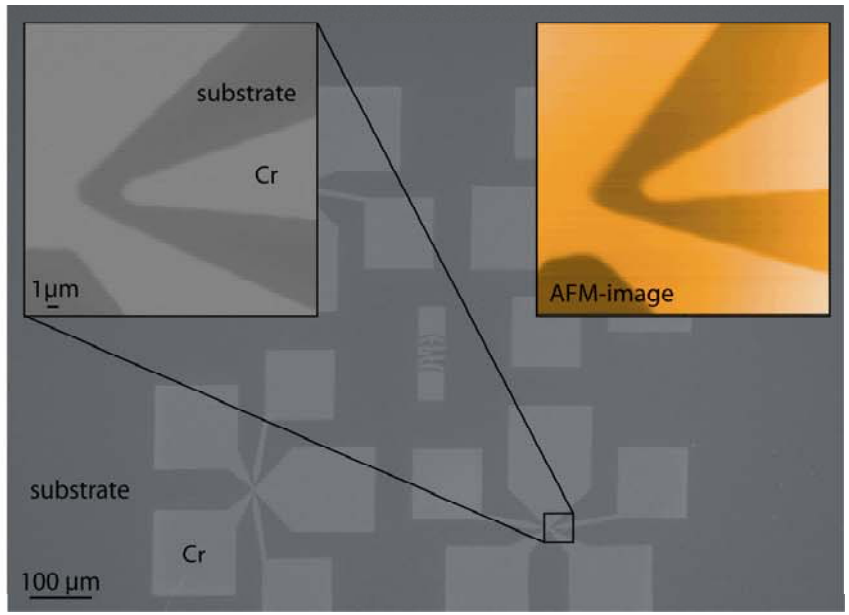


Improved Pattern transfer

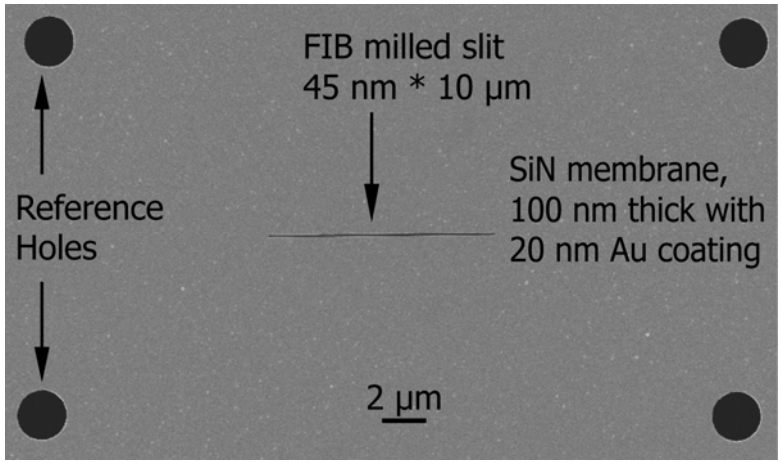
Surface pattern made by non-stabilized stencil



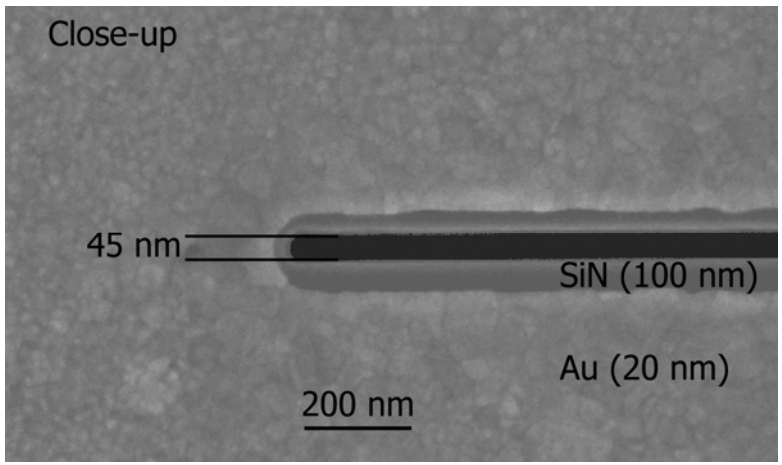
Surface pattern made by stabilized stencil

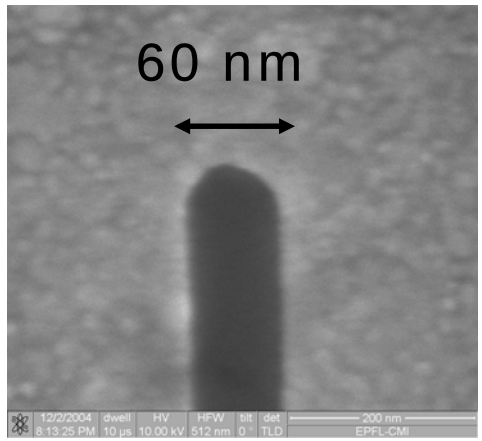


Nanostencils by FIB



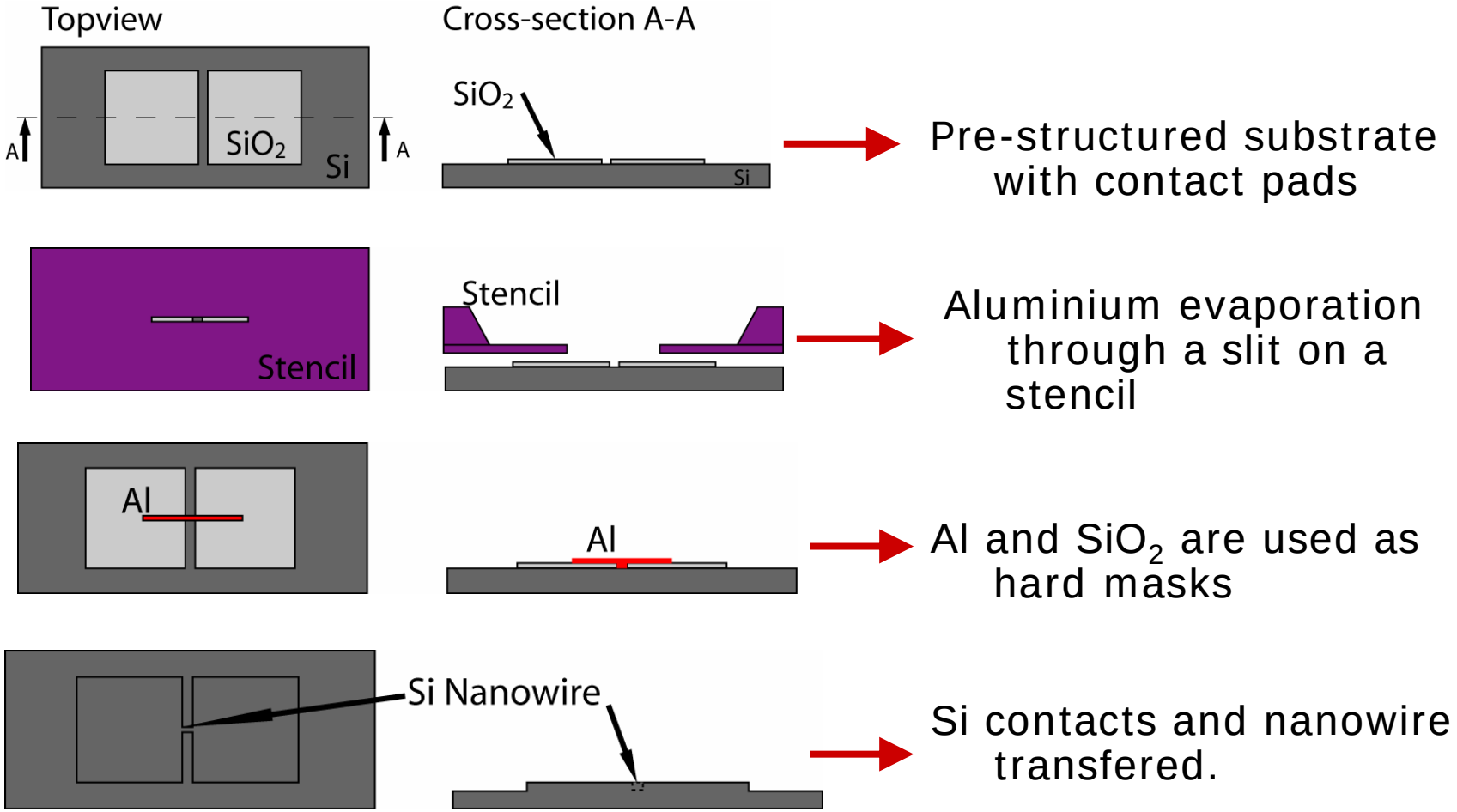
- SiN thickness: 100 nm
- Sub-100 nm width slits made by FIB
- Length: 10um
- 20 nm Au deposited on SiN to avoid charging during FIB



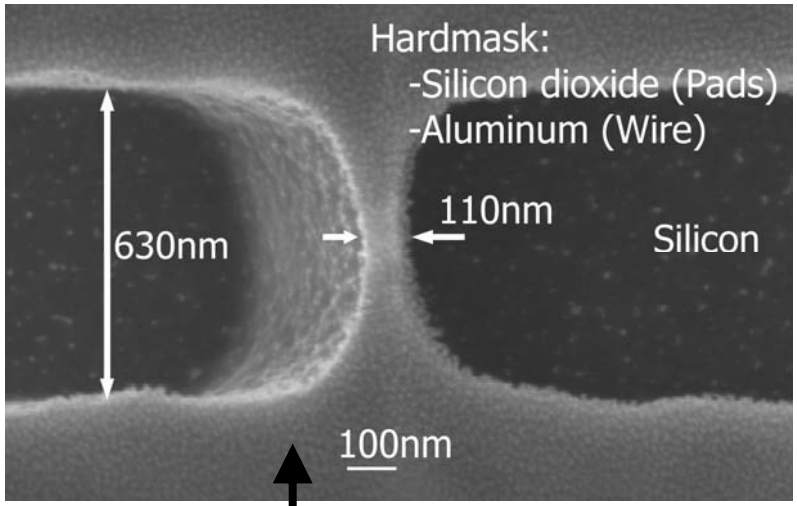


Applications for Micro and Nanoelectronics

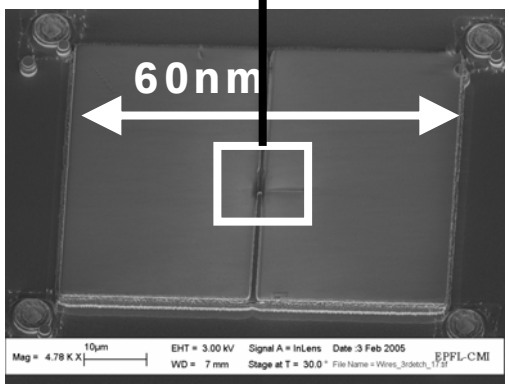
Nanowires based on Stencil Technique *(Developed by Daniel Grogg, now in LEG)*



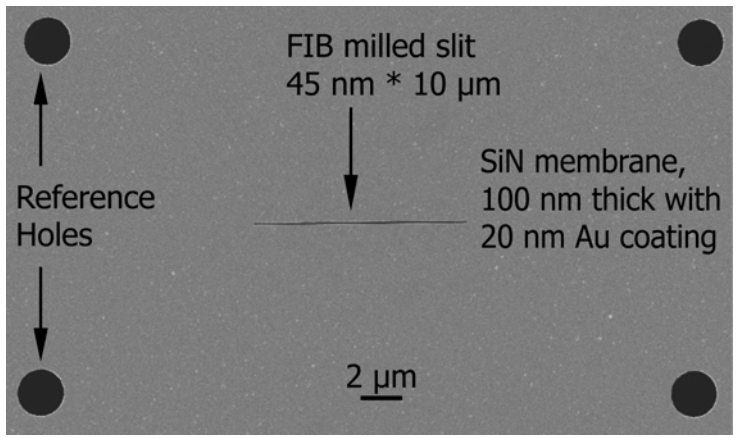
Applications for Micro and Nanoelectronics



Si Wire 110nm between contact pads after RIE etching.



Stencil fabricated with Photo-Litho and FIB



Applications for Micro and Nanoelectronics

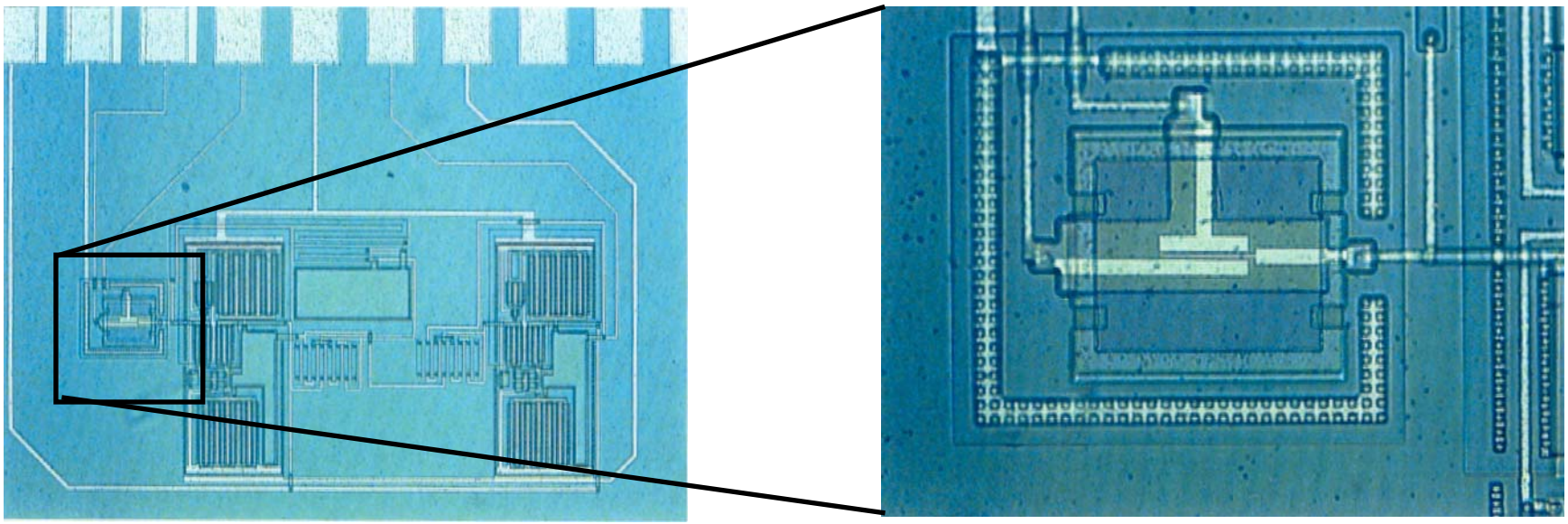
Outlook: Integration with CMOS technology and architectures

- Fabrication of Si wires <100 nm.
- I/V characterization (Temperature and Gate V)
- Develop CMOS/SiNW devices (with LEG, Prof. Ionescu)
- Fabrication NW/CMOS arrays (with LEG, Prof. Ionescu)
- Develop fault tolerant circuits (with LSM, Prof. Leblebici)

Nanoresonators on CMOS chip

in collaboration with Julien Arcamone CNM-CSIC, Institut de Microelectronica de Barcelona.

Nanostencil can be used for fabrication on pre-defined structures.



CMOS chip

Post-process: Al pattern using nanostencil

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